WE CLAIM

1. Apparatus for performing a saturating shift operation upon an input data value to generate an output data value, said apparatus comprising:

a data shifting circuit operable to shift an input data value by a shift amount dependent upon an input shift amount to generate a shifted data value;

a mask generating circuit operable to generate a mask value; and

a masking circuit operable to apply said mask value to said shifted data value to generate said output data value; wherein

said mask generating circuit operates in parallel with said data shifting circuit to detect in dependence upon said input data value and said input shift amount if said output data value should be saturated and, if said output data value should be saturated, then generates a mask value to control said masking circuit to generate a saturated data value as said output data value.

2. Apparatus as claimed in claim 1, wherein said data value shifting circuit is a data value rotating circuit operable to rotate an input data value by a rotation amount dependent upon an input shift amount to generated a rotated data value as said shifted data value and, if said output data value should not be saturated, then said mask generating circuit generates a mask value to control said masking circuit to generate a shifted data value not outside of saturating limits as said output data value.

3. Apparatus as claimed in claim 1, wherein said mask value is also operable to control sign extending of said output data value.

4. Apparatus as claimed in claim 1, wherein said mask generating circuit is responsive to a partially shifted data value to detect if said output data value should be saturated.

5. Apparatus as claimed in claim 1, wherein said masking circuit is a combinatorial logic array.

6. Apparatus as claimed in claim 1, wherein data value rotating circuit and said masking circuit are operable to reduce data width of said input data value when generating said output data value.

7. Apparatus as claimed in claim 6, wherein said mask generating circuit detects if said output data value should be saturated in dependence upon said input data value before data width reduction.

8. Apparatus as claimed in claim 1, wherein said apparatus is operable to perform a plurality of separate saturating shift operations in parallel upon respective portions of said input data value as part of single instruction multiple data operation.

9. Apparatus as claimed in claim 1, wherein said mask values are mask values divided into at least one of a run of binary ones and a run of binary zeros.

10. Apparatus as claimed in claim 1, wherein one or more control signals switch said apparatus between modes providing at least one of:

saturating operation or non-saturating operation;

signed output generation or non-signed output generation; and

narrowing or non-narrowing output generation.

11. A method of performing a saturating shift operation upon an input data value to generate an output data value, said method comprising the steps of:

shifting an input data value by a shift amount dependent upon an input shift amount to generate a shifted data value;

generating a mask value; and

masking said shifted data value with said mask value to generate said output data value; further comprising the step of:

in parallel with said shifting, detecting in dependence upon said input data value and said input shift amount if said output data value should be saturated and, if said output data value should be saturated, then generating a mask value to control said masking to generate a saturated data value as said output data value.

12. A method as claimed in claim 11, wherein said data value shifting circuit is a data value rotating circuit operable to rotate an input data value by a rotation amount dependent upon an input shift amount to generated a rotated data value as said shifted data value and, if said output data value should not be saturated, then said mask generating circuit generates a mask value to control said masking circuit to generate a shifted data value not outside of saturating limits as said output data value.

13. A method as claimed in claim 11, wherein said mask value is also operable to control sign extending of said output data value.

14. A method as claimed in claim 11, wherein said mask generation is responsive to a partially shifted data value to detect if said output data value should be saturated.

15. A method as claimed in claim 11, wherein said masking is performed by a combinatorial logic array.

16. A method as claimed in claim 11, wherein data width of said input data value is reduced when generating said output data value.

17. A method as claimed in claim 16, wherein detecting if said output data value should be saturated in dependence upon said input data value is performed before said data width is reduced.

18. A method as claimed in claim 11, wherein a plurality of separate saturating shift operations are performed in parallel upon respective portions of said input data value as part of single instruction multiple data operation.

19. A method as claimed in claim 11, wherein said mask values are mask values divided into at least one of a run of binary ones and a run of binary zeros.

20. A method as claimed in claim 11, wherein one or more control signals switch said between modes providing at least one of:

saturating operation or non-saturating operation;

signed output generation or non-signed output generation; and

narrowing or non-narrowing output generation.